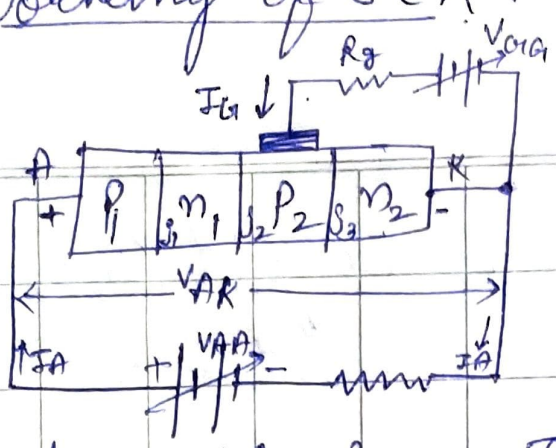
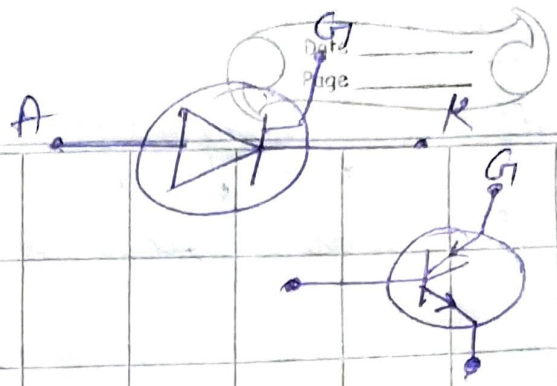
Working of SCR.

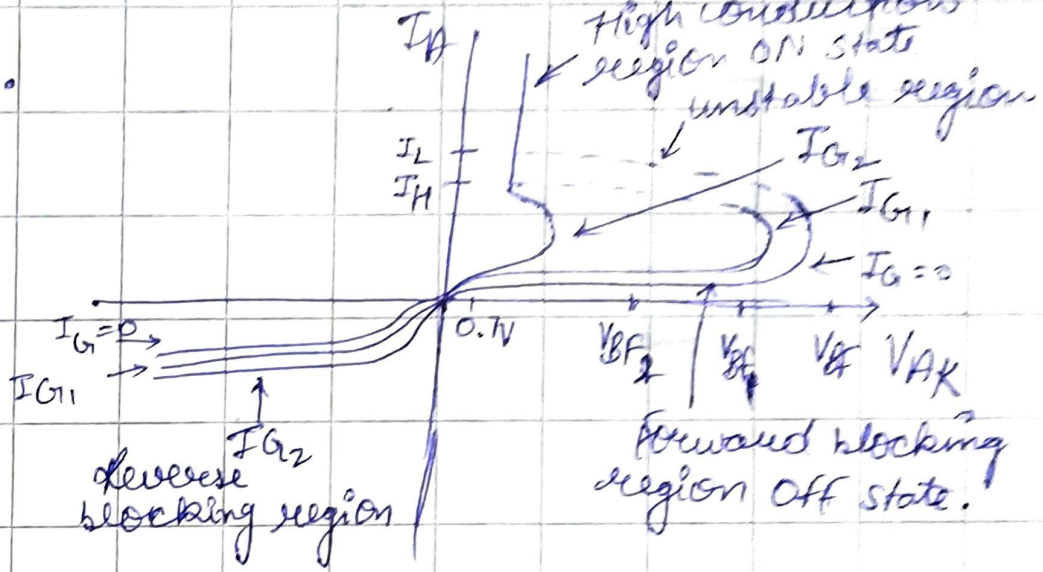




(1) Low biasing :- $I_G = 0$, forward blocking state., both tr. in Off state. Only I_{CO} (leakage current).

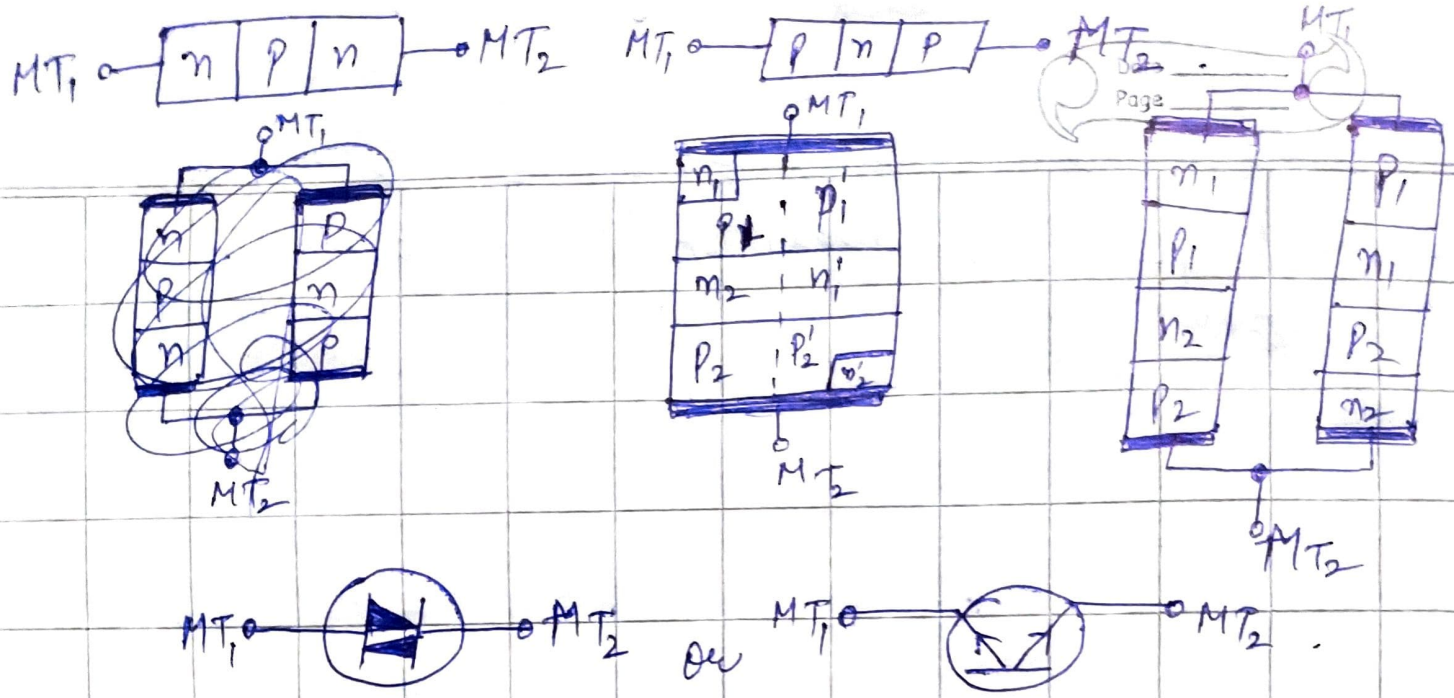
(2) High biasing :- When V_{AK} is low, $I_G = 0$, but as soon $I_G \neq 0$ i.e. it is made to flow into P_2 which is equivalent to supply holes into base P_2 of transistor Q_2 which makes J_3 forward biased. This causes supply of electrons from n_2 to P_2, further from J_2 to n_1 of Q_1 etc. This arrival of es initiates the injection of holes from P_1 to n_1. This causes both transistors to come into ON state and whole pnpn device is in forward conducting state. This gate triggering of device or device is said to be fixed. $I_G = mA$ and $I_A \geq 10^n A$.

When I_{G1} is made zero, SCR still conducts heavily, also voltage drop across anode to cathode is so small. The condition of SCR to remain in ON stage even when I_{G1} is made zero is latching.



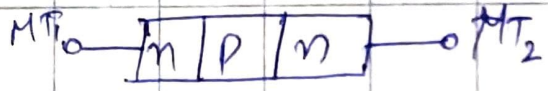
DIAC (Diode AC switch). (bidirectional semiconductor device which has on and off state for positive and negative anode voltages. used for triggering triacs. Two constructions :- (i) ac trigger diode (ii) bidirectional pnpn diode switch.

ac trigger diode → Similar to BJT except the doping conc. is same & no contact for base. It is two terminal device. It is actually pnpn shockley diodes connected in antiparallel to each other.

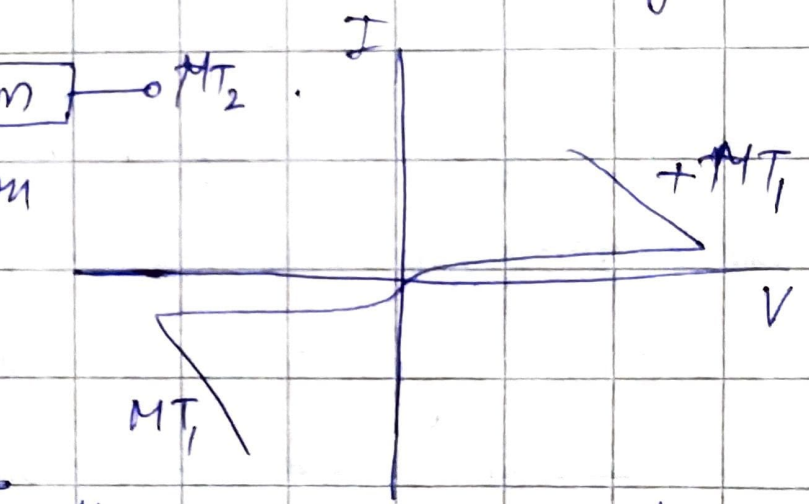


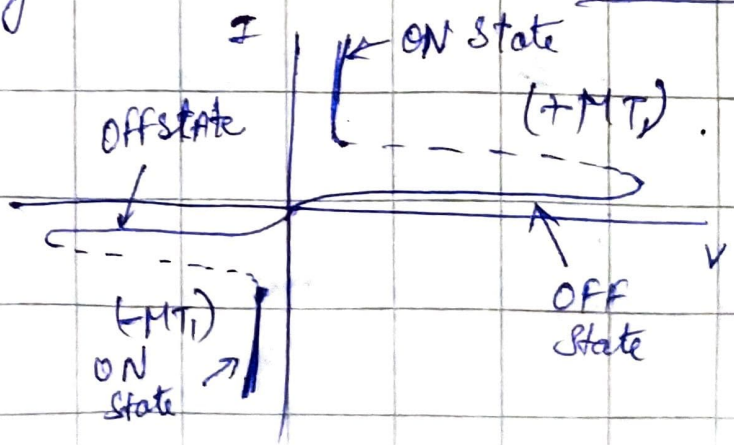
Symbol of DIAC

refereed to as triac without without gate terminals.



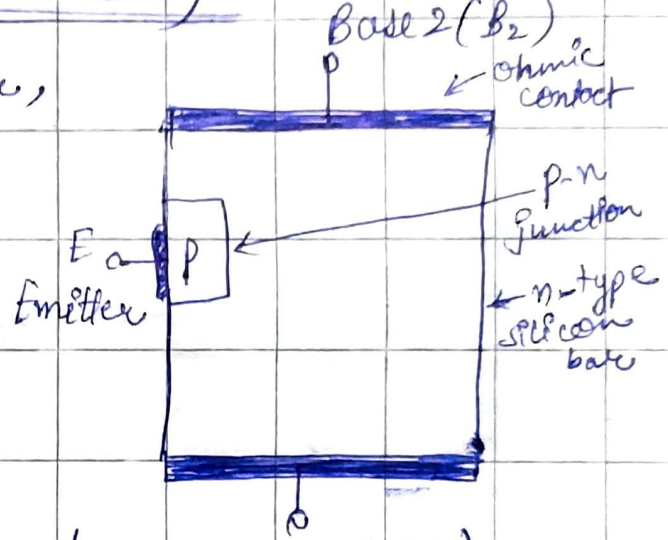
* This can be turned on ~~when~~ by both half cycles of ac voltage but if this applied voltage is more than forward breakover voltage. Below this, only small leakage current flows due to drift of holes and is at depletion layer. Diac remains in blocking state.



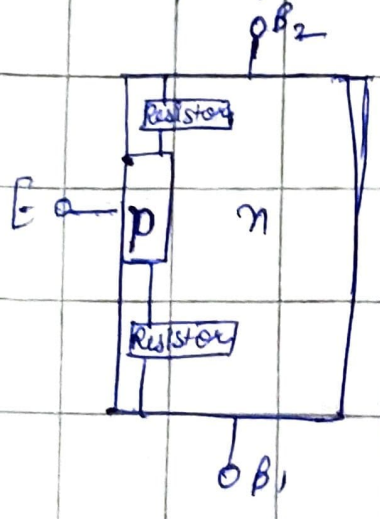


applied voltage > breakover voltage, in conducting state, voltage drop decreases, symmetrical in first and third quadrant for positive half cycle & negative half cycle of ac resp. It has larger negative resistance and smaller forward drop. breakover voltage range 30 - 40 V & time ranges (turn on) b/w 50 ns to 500 ns.

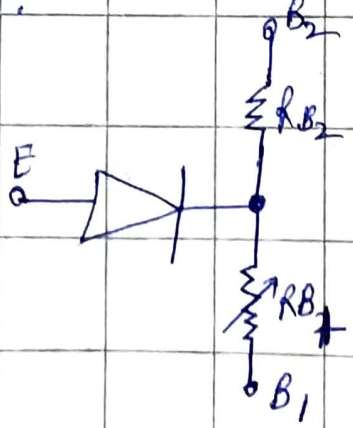
UJT (Uni - Junction Transistor)

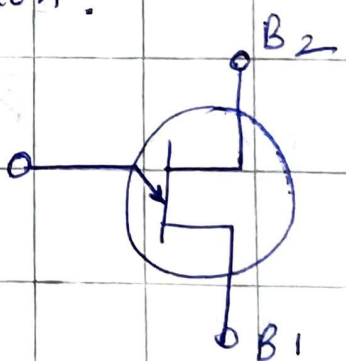


* lightly doped n-type silicon bar, heavily doped p-type region formed by diffusion of accepted type impurities on p-type material is alloyed.
E is close to B_2.
* Device shows that forward biased current goes from p-type to n-type region.
Also, we can have n-type emitter and p-type bar.



Or

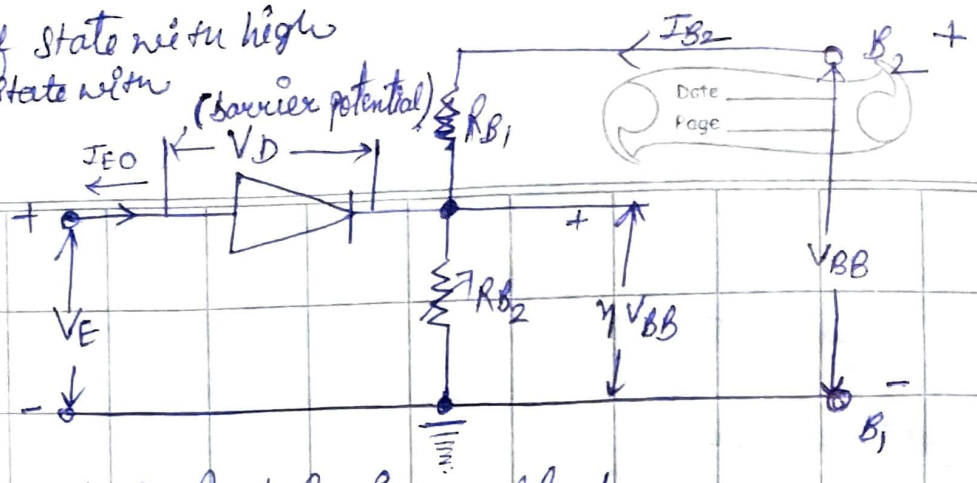




Symbol of UJT.

R_{B_1} is variable as it depends upon V_D, bias voltage or emitter current I_E.

two states → Off state with high impedence & ON state with low impedence.



The resistance b/w B_1 & B_2 is called

* <u>interbase resistance</u>. $R_{BB} = R_{B_1} + R_{B_2}$

no voltage, can measured by ohmmeter. R_{BB} lies b/w 4000 Ω to 10000 Ω. R_{B_1} is 60% of R_{BB}.

① <u>When E is open</u> :- V_{BB} divide across R_{B_1} & R_{B_2}, a fraction of this appears across R_{B_1} written as ηV_{BB}.

$$\eta V_{BB} = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} \times V_{BB}$$

$$= \frac{R_{B_1}}{R_{BB}} \times V_{BB} \Rightarrow \boxed{\eta = \frac{R_{B_1}}{R_{BB}}}$$

η is known as * <u>intrinsic staff off ratio</u>. value lies b/w 0.51 to 0.82.

② <u>$V_E < \eta V_{BB}$</u> :- then emitter junction becomes reverse biased & only small reverse current I_{EO} flows through it.

③ <u>$V_E > \eta V_{BB}$</u> :- Keeping V_{BB} fixed, we go on increasing V_E so that it exceeds ηV_{BB}, the emitter junction become forward biased, p-type start injecting holes to n type, decrease in resistance

b/w E & B_1 i.e. conductivity increases. then voltage drop across R_{B_1} reduced & thus emitter junction heavily forward biased, increased current, more charge carriers, reduction of resistance of R_{B_1} region. This is called * regenerative process. The process with which resistance varies is called * Conductivity modulation. There is * negative resistance effect. To make it off, V_E is made zero or input is open-circuited.

④ $V_E = \eta V_{BB}$:- then I_{E0} becomes zero, the junction is neither forward nor reverse bias.

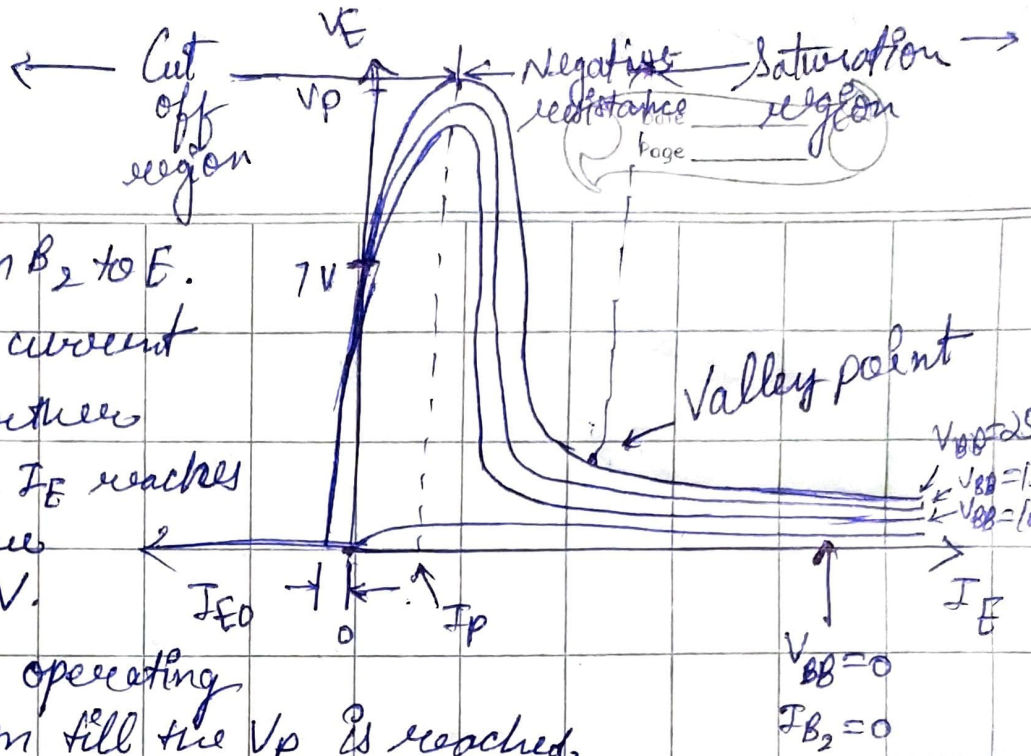
⑤ Peak voltage :- ηV_{BB} is reverse biased, the other factor that adds to this reverse bias is V_D (barrier potential) so total reverse bias voltage is $\eta V_{BB} + V_D$ then. for silicon $V_D = 0.7V$

V_P (Peak voltage) $= \eta V_{BB} + V_D$. $[V_D \simeq 5V]$.

When V_E exceeds this value, I_E starts flowing through R_{B_1}, b/w emitter & base 1. This is minimum current that would trigger UJT. Also $I_P \propto \frac{1}{V_{BB}}$.

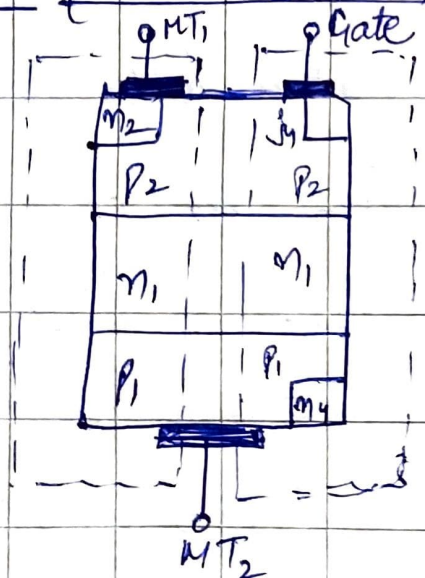
when UJT is forward biased, I_{B_2} current also increases and an external limiting resistance R_2 is connected is series to tr. with B_2.

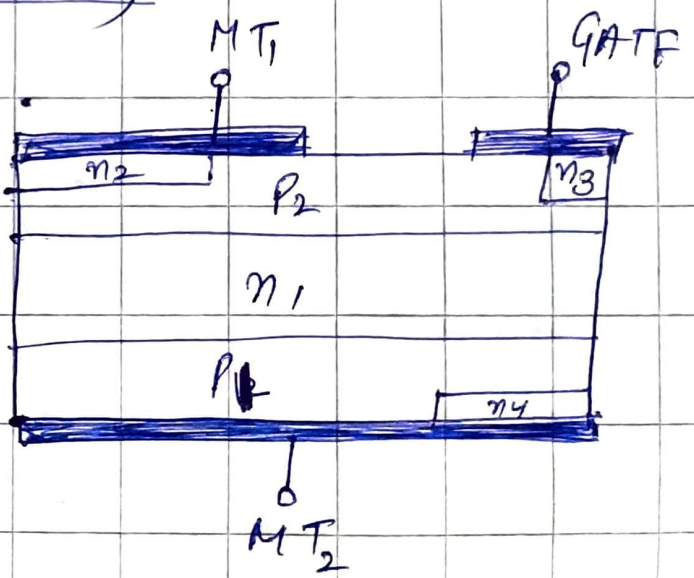
For $V_{BB}=0$, V_E results in I_E. There is leakage current I_{E0} from B_2 to E. When $V_E \simeq 7V$, the current reduced to 0 & further Increase in V_E, the I_E reaches to peak point value V_p shown for 25 V. UJT is said to be operating in cut off region till the V_p is reached. Corresponding to peak current I_p.

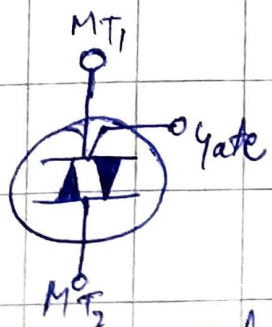


VI characteristics of UJT

TRIAC (Triode AC Switch)







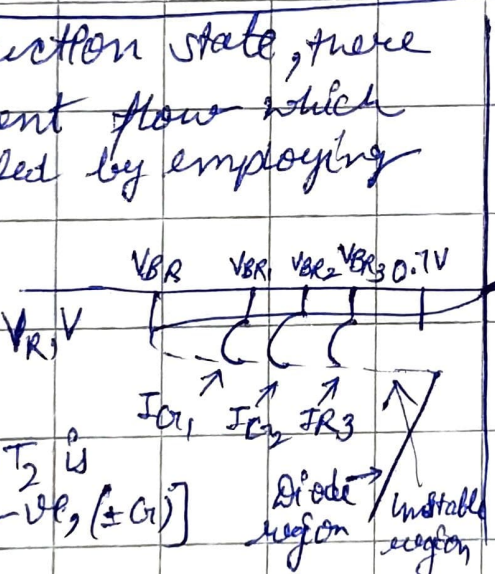
Symbol for triac.

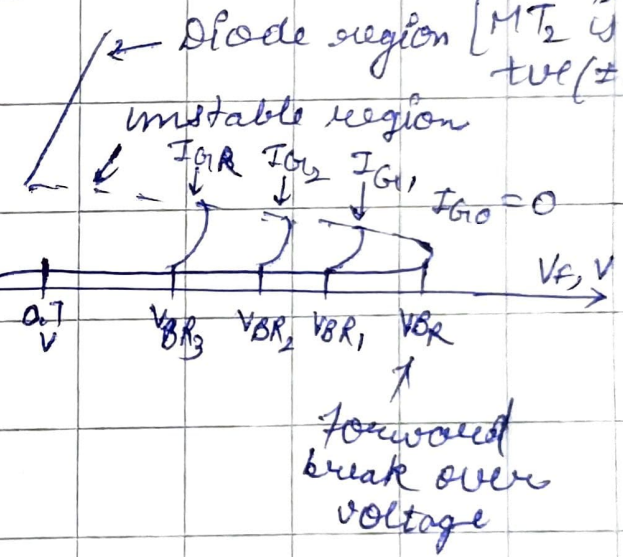
As we Increase gate current, the breakdown voltage ~~Increases~~ decreases.

After V_p, R_B, decreases due to ~~increase in~~ I_E injection of charge carriers from emitter, ~~to a sudden increase in~~ I_E is seen with decrease in V_E and device enter into negative resistance region. Conductivity modulation, unstable region. Here R_B, falls to a saturation resistance value R_s & this region lasts until valley voltage V_v is reached (I_v valley current).

$$V_E = V_D + I_E R_S$$

When in conduction state, there is large current flow which can be controlled by employing external resistances, otherwise device can destroy.





Different States :-

(i.) Forward blocking state – $MT_2 \rightarrow$ +ve wrt MT_1 but V is less than V_{BR} & gate is open (in forward).

(ii.) Reverse Blocking – When MT_2 -ve wrt MT_1 but V ① than V_{BR} & gate is open (in Reverse).

(iii-) Conduction State:- (ON state) if $V > V_{BR}$

gate open → Conduction.

Date _____

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